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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,119	11/21/2003	Douglas R. Hackler SR.	51889/3	1799

7590 06/15/2005

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/719,119	HACKLER ET AL.
	Examiner	Art Unit
	Phat X. Cao	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *14-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-13* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/22/04, 3/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I, claims 1-13 in the reply filed on 3/23/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, and 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al, "Super Self-Aligned Double-Gate (SSDG) MOSFETs Utilizing Oxidation Rate Difference and Selective Epitaxy", IEEE, pp. 3.5.1 – 3.5.4 (cited by Applicant) in view of Lehovec (US. 4,360,897).

Regarding claims 1 and 5, Lee (Figs. (e')-(f')) discloses a double-gate field effect Transistor including: a substrate; a bottom gate BG disposed on the substrate; a dielectric layer LTO disposed on the bottom gate BG and the substrate; a channel (i.e., Si film) disposed on the dielectric layer; a source disposed on the dielectric and having a source extension extending from the main body of the source and coupled to the channel; a drain disposed on the dielectric and having a drain extension extending from

the main body of the drain and coupled to the channel; a gate insulator disposed on the channel; a top gate TG disposed on the gate insulator; a first spacer disposed between the top gate TG and the source and proximate to the source extension; a second spacer disposed between the top gate TG and the drain and proximate to the drain extension.

Lee does not disclose the top gate TG coupled to a first input, the bottom gate BG coupled to a second input, and the drain coupled to an output.

However, Lehovec (Fig. 2a) teaches an OR gate circuit (column 3, lines 14-17) having a first gate coupled to a first input X, a second gate coupled to a second input Y, and a drain coupled to an output. Accordingly, it would have been obvious to connect the top gate and the bottom gate of Lee to the first input and the second input, and connect the drain to the output in order to form an OR gate circuit, as taught by Lehovec.

Regarding claims 2 and 6, Lee further discloses that the double-gated field effect transistor is a NMOS or PMOS (page 3.5.2, column 2, first paragraph).

4. Claims 1, 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al (US. 6,248,626) in view of Lehovec (US. 4,360,897).

Kumar (Figs. 4A-4F) discloses a double-gates field effect transistor including: a substrate 40; a bottom gate 45 disposed on the substrate; a dielectric disposed on the bottom gate and the substrate; a channel 48 disposed on the dielectric; a source disposed on the dielectric and having a source extension extending from the main body of the source and coupled to the channel; a drain disposed on the dielectric and having a drain extension extending from the main body of the drain and coupled to the channel;

a gate insulator 47 disposed on the channel; a top gate G disposed on the gate insulator; a first spacer 50 (left side) disposed between the top gate G and the source and proximate to the source extension; and a second spacer 50 (right side) disposed between the top gate G and the drain and proximate to the drain extension. Kumar further discloses that the channel 48 or layer 44 is undoped (i.e., silicon) (column 6, lines 8-11).

Kumar does not disclose the top gate coupled to a first input, the bottom gate coupled to a second input, and the drain coupled to an output.

However, Lehovec (Fig. 2a) teaches an OR gate circuit (column 3, lines 14-17) having a first gate coupled to a first input X, a second gate coupled to a second input Y, and a drain coupled to an output. Accordingly, it would have been obvious to connect the top gate and the bottom gate of Kumar to the first input and the second input, and connect the drain to the output in order to form an OR gate circuit, as taught by Lehovec.

5. Claims 5 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (US. 2002/0093053) in view of Kumar et al (US. 6,248,626) and Lehovec (US. 4,360,897).

Regarding claim 5, Chan (Figs. 1A –1C) discloses a double-gated field effect transistor including: a substrate 4; a bottom gate (not labeled) disposed on the substrate; a dielectric 3/11 disposed on the bottom gate an the substrate; a channel 5 disposed on the dielectric; a source 9 disposed on the dielectric; a drain 9 disposed on the dielectric; a gate insulator 11 disposed on the channel (see Fig. 1W); a top gate 12

disposed on the gate insulator 11; a first spacer 11 (corresponding to a portion of an insulating layer 11 formed on a left sidewall of the gate 12) (see Fig. 2AA and par. [0073]) disposed between the top gate 12 and the source 9 and proximate to the channel 5; and a second spacer 11 (corresponding to a portion of an insulating layer 11 formed on a right sidewall of the top gate 12) (see Fig. 2AA and par. [0073]).

Chan does not disclose the source/drain 9 having the source/drain extensions.

However, Kumar (Figs. 4E and 4F) teaches the forming of a dual-gate device comprising the source/drain disposed on a dielectric and having source/drain extensions extending under the top gate and coupled to the channel 48. Accordingly, it would have been obvious to modify the transistor of Chan by forming the source/drain 9 with the source/drain extensions as suggested because such source/drain extensions are well known and commonly used for preventing the short channel effect of the transistor.

Neither Chan nor Kumar disclose the top gate coupled to a first input, the bottom gate coupled to a second input, and the drain coupled to an output.

However, Lehovec (Fig. 2a) teaches an OR gate circuit (column 3, lines 14-17) having a first gate coupled to a first input X, a second gate coupled to a second input Y, and a drain coupled to an output. Accordingly, it would have been obvious to connect the top gate and the bottom gate of Chan to the first input and the second input, and connect the drain to the output in order to form an OR gate circuit, as taught by Lehovec.

Regarding claims 10-11, Chan (Fig. 1A) further discloses that the gate insulator 11 has a cross-sectional U-shape and the channel 5 is undoped (i.e., SOI).

Regarding claims 12-13, Chan (Fig. 2W) further discloses: a plurality of exterior spacers 11 disposed on the sidewalls of source/drain 9 and proximate to the dielectric layer 3, and source/drain 9 (corresponding to the portions of an insulating layer 11 formed on the side surfaces of source/drain 9), and an insulator 13 (Fig. 1A) disposed on the substrate and coupled to the exterior spacers 11.

6. Claims 5 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parke (US. 6,580, 137) in view of Hanafi et al (US. 2002/0105039) and Lehovec (US. 4,360,897).

Regarding claim 5, Parke (Figs. 12B and 12C) discloses a double-gated field effect transistor including: a substrate 11; a bottom gate 124' disposed on the substrate; a dielectric 13 disposed on the bottom gate and the substrate; a channel 122 disposed on the dielectric; a source 114s disposed on the dielectric; a drain 114d disposed on the dielectric; a gate insulator 128 disposed on the channel; a top gate 130 disposed on the gate insulator; a first spacer 30 disposed between the top gate and the source and proximate to the channel 122; and a second spacer 30 disposed between the top gate and the drain and proximate to the channel 122.

Parke does not disclose the source/drain 114 having the source/drain extensions.

However, Hanafi (Fig. 10) teaches the forming of a dual-gate device comprising the source/drain disposed on a dielectric 24 and having source/drain extensions 32

extending under a top gate 46 and coupled to the channel 40. Accordingly, it would have been obvious to modify the transistor of Parke by forming the source/drain 114 with the source/drain extensions as suggested because such source/drain extensions are well known and commonly used for preventing the short channel effect of the transistor.

Neither Parke nor Hanafi disclose the top gate coupled to a first input, the bottom gate coupled to a second input, and the drain coupled to an output.

However, Lehovec (Fig. 2a) teaches an OR gate circuit (column 3, lines 14-17) having a first gate coupled to a first input X, a second gate coupled to a second input Y, and a drain coupled to an output. Accordingly, it would have been obvious to connect the top gate and the bottom gate of Park to the first input and the second input, and connect the drain to the output in order to form an OR gate circuit, as taught by Lehovec.

Regarding claims 12-13, Parke (Fig. 12B0 further discloses: a plurality of exterior spacers 30 (not labeled, see Fig. 13B) disposed on the substrate 11 and proximate to the dielectric layer 13, and source/drain 144, and an insulator layer 40 (Fig. 9B) disposed on the substrate and coupled to the exterior spacers 30.

7. Claims 3-4 and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al and Lehovec as applied to claims (1,5) above, and further in view of Gunderson et al (US. 2004/0083435).

The combination of Lee and Lehovec does not disclose a precharge transistor coupled to the drain (output) of the OR gate.

However, Gunderson (Fig. 2) teaches the forming of an OR gate circuit 20 comprising a precharge transistor 21 coupled to the drain (output) of the OR gate. Accordingly, it would have been obvious to couple the drain of the OR gate of the above combination to the precharge transistor in order to assist in charging storage node to the appropriate/desired charge/value, as taught by Gunderson (par. [0016]).

Gunderson (Fig. 2) also discloses a NMOS transistor is used for the OR gate circuit and a PMOS transistor is used for the precharge circuit. Therefore, it would have been obvious to convert the NMOS OR gate to the PMOS OR gate and the PMOS precharge transistor to the NMOS precharge transistor because the NMOS transistor is analogous to the PMOS transistor, with the transistor operational polarity and doping types reversed.

8. Claims 3-4 and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al and Lehovec as applied to claims (1,5) above, and further in view of Gunderson et al (US. 2004/0083435).

The combination of Kumar and Lehovec does not disclose a precharge transistor coupled to the drain (output) of the OR gate.

However, Gunderson (Fig. 2) teaches the forming of an OR gate circuit 20 comprising a precharge transistor 21 coupled to the drain (output) of the OR gate. Accordingly, it would have been obvious to couple the drain of the OR gate of the above combination to the precharge transistor in order to assist in charging storage node to the appropriate/desired charge/value, as taught by Gunderson (par. [0016]).

Gunderson (Fig. 2) also discloses a NMOS transistor is used for the OR gate circuit and a PMOS transistor is used for the precharge circuit. Therefore, it would have been obvious to convert the NMOS OR gate to the PMOS OR gate and the PMOS precharge transistor to the NMOS precharge transistor because the NMOS transistor is analogous to the PMOS transistor, with the transistor operational polarity and doping types reversed.

Allowable Subject Matter

9. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art fails to disclose the channel has a cross-sectional U-shape.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
June 10, 2005

PHAT X. CAO
PRIMARY EXAMINER